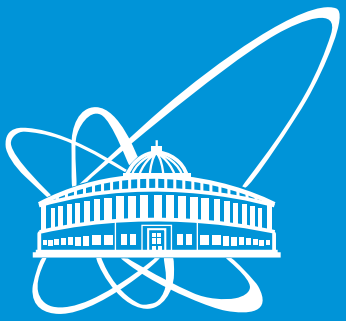

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MULTIGATE AND FAST CLEAR LOGIC IN **FERA** READOUT

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1. Introduction.

In the DIRAC experiment [1] at CERN readout of considerable part of the data is realized with the LeCroy FERA system [2] (Fast Encoding and Readout ADC). Four FERA branches are used in the experiment. They include FERA drivers 4301 and ADC 4300B originally designed for the FERA readout system and two types of FERA compatible modules: TDC 3377 and universal logic modules 2366.

In total the FERA readout system in DIRAC includes 15 ADC 4300B, 22 TDC 3377, 4 modules 2366 and 4 (one per branch) FERA drivers 4301. The programmable universal logic modules 2366 have been configured [3] in this application like FERA registers and scalers. During the accelerator burst the events are transferred to 4 VME buffer memories CES 8170 which have the volume sufficient to store all the data accumulated in one burst. The readout [4] of the buffer memories' content to the VME processor board takes place in the interval between the bursts.

Below we describe the operation of FERA readout using several different gates in the same branch and several sources of clear. The modules of different types can be mixed within the same FERA branch. Note that some minor but important modifications should be done in universal logic modules 2366 for their FERA compatibility[1].

2. Multiple gating.

The reasons to use different gates in the same FERA branch could be numerous, for example, a necessity to have a distinct gate width or gate delay for the modules of some detectors. In the DIRAC experiment there are additional arguments in favour of different gates. It can be elucidated by a much simplified scheme of the setup in Fig.1 (see [5] for more detailed scheme). The setup consists of a target, a spectrometric magnet, and detectors upstream of the magnet and in two arms in the downstream part. For most of the detectors the timing information is read out and for some of them the amplitude information, too.

[1]The module 2366 has no ground pin in the FERA control connector (all inputs and outputs of this module are differential ECL). Meanwhile two of the FERA control signals, WST and REQ, must be configured as single-ended. To achieve electrical compatibility the ground plane of the module 2366 should be connected to the negative pins of the WST and REQ outputs of this module.

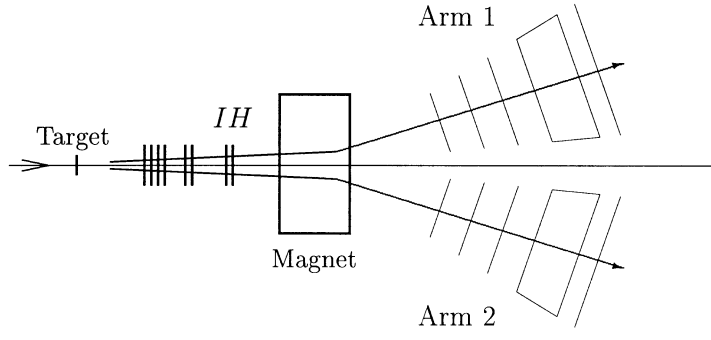

Fig.1. Experimental layout.

The data analysis in DIRAC requires collection of not only real coincidences of π^+ and π^- in two arms but also their accidental coincidences up to $\Delta t = \pm 20\, ns$ difference in timing of two arms. The use of a common gate in both arms would require a wider gate to have some margins for taking these accidentals. In contrast, if the gate to the modules of the detectors in one arm is synchronized with timing of a particle in the same arm, then the gate width may be narrower and the background (due to pile-up) is decreased. For this reason three types of gates are applied: synchronized with Arm 1, synchronized with Arm 2 and non-synchronized. The non-synchronized gate is produced directly by the first level trigger [5] and is applied mainly to the upstream detectors where such synchronization has no advantage. The synchronized gates are produced through the coincidences of the first level trigger with the signal resulting from the detector coincidences within one corresponding arm.

The practical realization of the multi-gate FERA operation is shown in Fig.2. The readout modules in the crate are grouped in accordance with the gate type to be applied. The non-synchronized "Gate 1" comes to a gate input of a FERA driver and is distributed via the FERA control bus to the modules of the first group. On passing the last module in the group the "Gate" line of the control bus is cut and proper ter-

mination of this line is executed externally. The signals "Gate 2" and "Gate 3" are the gates synchronized with a particle in Arm 1 or Arm 2, respectively. Missing a FERA driver these signals are applied directly to the "Gate" lines of the corresponding sections. The "Gate 2" line is also terminated externally while termination of the 3-rd section is executed in a standard way with terminating resistor array inside the last module.

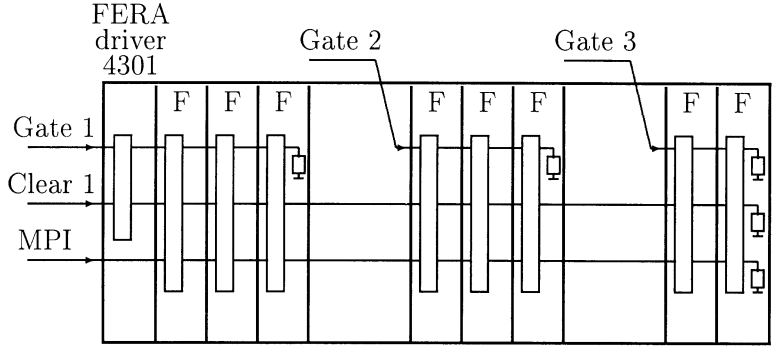

Fig.2. FERA control bus with multiple gating.
"F" denotes any FERA compatible module.

The Clear signal is common for all the modules in this crate and is distributed through the FERA driver and the control bus as usual. The purpose of the MPI line is discussed in Section 4.

Some of the ADCs operate in a self-Clear mode. A gate and clear technics for this case is described below.

3. Gate commutation and self-Clear.

Two more gates are applied in a special way only to ADCs of the ionization hodoscope IH. This scintillation hodoscope is used in particular in the second level trigger for selection of double ionization events, i.e. events with two charged particles crossing the same hodoscope counter. As always in this experiment, the equivalent conditions for real and ac-

cidental coincidences should be provided in any applied cut. In the IH case this means that the double ionization threshold should affect detection of two accidental particles (within the chosen coincidence width) in the same way as detection of real pairs. This can be achieved with integration of signals before discrimination.

Integration of signal charges was realized in a modified FERA ADC 4300B [6]. The modified modules keep all the features of a standard ADC 4300B but include also an implemented circuit which integrates the input charges within the gate width and sends the output signals to the ADC front panel for further discrimination.

The gates to IH ADCs are produced by a pretrigger T0 which is $\sim$ 200 ns earlier than the master trigger T1 (which starts the event acquisition) and has the rate 10–20 times higher than T1. The charge latched in the ADC and received by the integrator should be cleared if T0 is not accompanied by the master trigger T1. As the time around 2 μs is needed to clear the module, this process inserts a dead time which is of several percent in real experimental conditions.

To reduce this dead time the number of ADCs for IH was doubled and the gates were distributed between two groups of the modified ADCs using a dedicated Commutator unit. On receiving the T0 pretrigger, the Commutator sends a gate to the first group of ADCs and simultaneously sets a Busy interval. If the next T0 comes during the Busy signal, the Commutator redirects the new gate to the second ADC group and sets a second Busy. In this scheme the dead time is decreased practically to zero as it appears only if the third T0 is generated while both Busy signals are active.

The FERA control bus arrangement for this case is shown in Fig.3. As in Fig.2, the gate produced by the master trigger ("Gate 1") is distributed via the FERA driver and the first part of the control bus while the signals "Gate 4" and "Gate 5" from the Commutator come to the intercuts of the control bus "Gate" line in proper places. If the interval between the two consequtive triggers T0 exceeds the Busy signal duration, then only "Gate 4" is active. Otherwise the second T0 causes the gate signal at the "Gate 5" input.

The Clear signals are also different in this case. "Clear 1" is a usual clear signal common for all readout modules. One more kind of Clear – "self-Clear" – is applied to IH ADCs. The self-Clear signal is issued if the master trigger T1 did not come in the expected time (i.e. in 200 ns

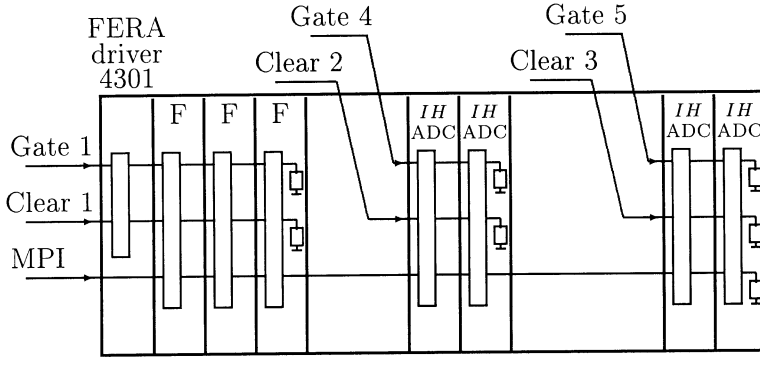

Fig.3. FERA control bus for the gate commutation and self-Clear operation mode.

after T0). The source of the self-Clear is the Commutator which not only sends a gate to *IH* ADCs but also copies it to a time-out scheme which generates a self-Clear at the end of the time-out period. If the master trigger appears in time, the self-Clear signal is inhibited. As the number of T0 exceeds many times the number of master triggers, the self-Clear is applied after most gates.

The control bus "Clear" line is cut in the same way as the "Gate" line. The input signal "Clear 2" is an OR of a common Clear and "self-Clear 1" (Fig.4). A similar logic is arranged for "Clear 3"; here the signal "self-Clear 2" may arise only if the Commutator has selected the second *IH* ADC group for gating (i.e. if "Gate 5" is active).

The above scheme with the gate commutation and implemented self-Clear was successfully used during the first year of the experiment running[2].

[2]Later the integrators on the basis of the modified ADC were replaced by dedicated integrators with a smaller dead time. The commutation scheme was removed and only one group of *IH* ADCs is now in operation. Nevertheless, the logic of gating and clearing of these ADCs is the same: a separate gate from the pretrigger T0 and a self-Clear applied if no master trigger is produced.

4. Fast clear.

The DIRAC trigger is a multilevel system which selects events taking into account the properties of the process in study. To detect $\pi^+\pi^-$ atoms (measurement of their lifetime is the goal of the experiment) one has to suppress pion pairs with high relative momenta Q at the trigger level. Therefore at all trigger stages the selection criteria cutting high Q values (or some of its components Q_x, Q_y, Q_L) are involved.

The high level hardware trigger processors T3 [7] and T4 take their decisions to accept or to reject the event when digitization in ADC and TDC is already in progress. If the decision of any of these processors is negative, the event is rejected and the data in the modules should be cleared. The processing of the event in ADC 4300B may be interrupted at any time. In contrast, in TDC 3377 the Clear signal during acquisition is effective only within a Measure Pause Interval (MPI). Hence, the MPI duration should be matched with the decision time of T3 and T4. The MPI is started by a Common Stop signal (a master trigger in our case) and the MPI value may be either fixed in software and loaded via a CAMAC bus or set via the front panel. In the latter option the MPI is equal to the signal duration at the front panel MPI input.

The T3 processor applies a cut to a relative momentum in a particle pair using hit maps of the IH detector and of two scintillation hodoscopes in the downstream arms. It has a fixed decision time of 120 ns. The processing time of T4, which reconstructs the tracks in the drift chambers, depends on the complexity of the event and, being in average around $2\,\mu s$, may sometimes exceed $10\,\mu s$. The maximum value for the software setting of MPI is $3.2\,\mu$s, which is not always sufficient for T4 decision. For this reason the MPI interval is set in hardware using the front-panel MPI input of the TDC 3377 modules. The externally applied MPI starts simultaneously with receiving the gate and is released after the T4 operation is completed. Thus, the Clear signal becomes effective at any stage of event processing. In practice, the MPI signal is sent to the modules via the control bus extended from 2x8 to 2x10 lines (see Fig.2 or 3). As the FERA driver has only 2x8 pins connector for the control bus, the bus extension begins after the FERA driver and the MPI signal comes directly to the extended part. The MPI line in the control bus by-passes the FERA modules of other than TDC 3377 types.

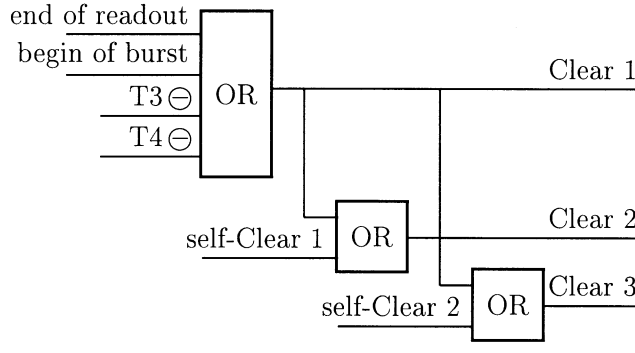

Fig.4. Logic of Clear applied to FERA modules.

The logic of Clear for the FERA branches is shown in Fig.4. Different sources of Clear are properly OR'd before sending to the control buses. Clear after the end of readout is a standard command after the data transfer, it does not interrupt the event processing. Clear at the beginning of the accelerator burst (added for reliable "ready" status after the software operations between the bursts) is a similar one. It is initiated by the leading edge of the accelerator spill. The rest of the sources of Clear – negative decisions of T3 or T4, self-Clear – produce fast Clear signals which may come at any time during the event processing.

Stable operation of the described scheme confirms that multi-gate and fast clear logic allows a flexible readout system with different FERA compatible modules to be created for multilevel trigger applications.

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Логика считывания FERA с использованием множественных сигналов Gate и Clear

Описывается организация считывания FERA с несколькими источниками сигналов Gate и Clear в одной и той же ветви, в том числе быстрого сигнала Clear до завершения оцифровки или передачи данных. В ветви применяются FERA-совместимые модули КАМАК различных типов. Представленная логика реализована в эксперименте ДИРАК с четырьмя FERA-ветвями.

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Multigate and Fast Clear Logic in FERA Readout

The operation of CAMAC FERA readout with several sources of Gate and Clear signals in the same branch is described including fast Clear before completion of the digitization or the data transfer. Different FERA compatible modules are used within the branch. The presented logic is implemented in the DIRAC experiment with four FERA branches.

The investigation has been performed at the Dzhelepov Laboratory of Nuclear Problems, JINR.

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